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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/667,388	09/23/2003	Terry R. Lee	M4065.0007/P007-B	9379

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EXAMINER	
BONZO, BRYCE P	

ART UNIT	PAPER NUMBER
2114	

DATE MAILED: 08/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/667,388	LEE, TERRY R.	
	Examiner	Art Unit	
	Bryce P. Bonzo	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *59-83* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *65 and 77-83* is/are allowed.

6)☒ Claim(s) *59-64,71 and 72* is/are rejected.

7)☒ Claim(s) *66-70 and 73-76* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

NON-FINAL OFFICIAL ACTION

Status of the Claims

Claims 59-67, 71 and 72 are rejected under 35 USC §102.

Claims 65 and 77-83 are allowed.

Claims 66-70 and 73-76 are objected to while containing allowable subject matter.

Objections to the Claims

Claims 60-64 and 66-70 are objected to as they have a dependency error. These claims all depend from claims 60 or 66, including 60 and 66. For purposes of examination claims 60 and 66 are determined to be depending from 59 and 65, respectively. Appropriate correction is required.

Rejections under 35 USC §102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 59-67, 71 and 72 are rejected under 35 U.S.C. 102(b) as being anticipated by Collins (United States Patent No. 4,564,943).

As per claim 59, Collins discloses:

A method of generating a latency drift signal comprising the steps of:

generating a first signal for indicating that data requested has been received (column 5, lines 1-4);

generating a plurality of derivative signals from said first signal, said plurality of derivative signals corresponding to a plurality of states of said first signal at a respective plurality of times (Figures 11 A-D);

comparing at least two of said derivative signals (Figure 10); and

generating a latency drift signal when said at least two of said derivative signals exhibit a predetermined relationship (column 10, lines 22-26).

As per claim 60, Collins discloses:

inputting said plurality of derivative signals into a plurality of delay circuits (Figure 6; column 5, lines 5-30).

As per claim 61, Collins discloses:

wherein said at least two of said derivative signals are compared using an OR gate (column 12, lines 25-31).

As per claim 62, Collins discloses:

wherein the latency drift signal is used to determine a latency drift in a memory circuit (column 3, lines 47-59).

As per claim 63, Collins discloses:

wherein said derivative signals are delayed relative to said first signal (column 5, lines 1-30).

As per claim 64, Collins discloses:

wherein each of said derivative signals is delayed relative to a preceding derivative signal (column 5, lines 1-30).

As per claim 71, Collins discloses:

A latency drift detector comprising:

means for receiving a ready signal of a programmable response time memory component whose response time is being measured (column 5, lines 1-4).

As per claim 72, Collins discloses:

a messaging means for indicating to a user a status of said memory component (column 10, lines 1-26).

Allowable Subject Matter

Claims 65 and 77-83 are allowed.

Claims 66-70 and 73-76 are objected while containing allowable subject matter.

Applicant is reminded that Allowable subject matter is indicated based on the claims as a whole including any intervening base claims. Provided below is an indication of the limitations which in combination with the remainder of the claim overcome the prior art.

As per claims 65-70:

A method of generating a latency drift signal comprising the steps of:

receiving a master clock signal at a first clock input of a latency detection circuit, said master clock signal being adapted to indicate a first start time of a signal response window, said response window including a first time interval of first duration;

receiving a transaction status signal at a second transaction status input of said latency detection circuit during said first time interval;

sampling a state of said transaction status signal with said latency detection circuit at a plurality of sampling times with said first time interval; and

receiving a latency status signal from said latency detection circuit at a control device, said latency status signal corresponding to a state of said transaction status signal at one or more of said plurality of sampling times.

As per claim 73:

wherein said determining means utilizes long term averaging.

As per claim 74:

wherein said determining means utilizes short term averaging.

As per claim 75:

wherein said determining means generates latency drift data for a plurality of memory components.

As per claim s 77-83:

77. A method of increasing reliability of an electronic system comprising:

receiving a master clock signal at a first clock input of a latency detection circuitry said master clock signal being adapted to indicate a first start time of a signal response window, said signal response window including a first time interval of a first duration;

receiving a transaction status signal at a second transaction status input of said latency detection circuit during said first time interval;

sampling a state of said transaction status signal with said latency detection circuit at a plurality of sampling times within said first time interval;

receiving a latency status signal from said latency detection circuit at a control device, said latency status signal corresponding to a state of said transaction status signal at one or more of said plurality of sampling times; and

servicing a component corresponding to said transaction status signal based on a state of said latency status signal received at said control device.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Bryce P. Bonzo whose telephone number is (571)272-3655. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571)272-3645. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Bryce P. Bonzo

Bryce P Bonzo
Primary Examiner
Art Unit 2114